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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,981	03/01/2004	Sanjay Bhardwaj	04303/000N238-US0	2112

20350 7590 12/14/2009

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EXAMINER	
AHMED, ENAM	

ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
12/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,981	BHARDWAJ, SANJAY	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-17 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non-Final

- This office action is in response to the applicant's RCE filed on 12/03/09.

Response to applicant's amendment

The applicant's arguments have been fully considered, however are not found persuasive.

Response to applicant's remarks

With respect to claim 10 on page 7, the applicant argues the Grivna reference does not teach a tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns.

The Examiner respectfully disagrees with the statement, and points out Grivna does teach, distributed framing – bit detection logic – 550, which is coupled to register 580, to force a bad parity signal, wherein the external bus is presented with a 19-bit character/pattern having invalid parity. Thus, the Grivna reference teaches tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns (column 10, lines 35-43).

With respect to claim 10 on page 7, the applicant argues Wright does not teach or suggest the searching of one frame sync pattern, let alone simultaneously monitoring two or more synchronization patterns.

The Examiner respectfully disagrees with the statement, and points out Wright does teach monitoring Frame Sync signal FS produced by the multiplexer. Thus, the Wright reference does teach monitoring synchronization pattern (column 5, lines 42-53).

With respect to claim 10 on pages 7-8, the applicant argues Kaufmann fails to teach or suggest a first, second, third, and fourth registers, the selector, the rotator, the select logic unit, the tester coupled to the fourth register for simultaneously monitoring two or more synchronization patterns.

The Examiner respectfully disagrees with the statement, and points out fig. 5 of Kaufmann, does have the above units or elements in a dynamic view.

With respect to claim 11, on page 8, the applicant argues while Swoboda discloses the term "exhausted" in relation to a "register", this term has a totally different meaning than the claimed exhausted register which keeps track of the bit positions already exhausted by the guesser.

The Examiner respectfully disagrees with the statement, and points Swoboda does teach, wherein a counter counts down until the number represented by the shift register is exhausted. Thus, the

Swoboda reference teaches an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser (column 38, lines 32-41).

35 U.S.C. 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 is rejected under 35 U.S.C. 112 2nd paragraph, due to the reasoning that claim 10 mentions a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output data word. However, it is not clear as to why a second output data word or a shifted data word is being selected, and secondly it is not clear from the claim as to where the shifted data word is generated from.

35 U.S.C. 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill

in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 13-17, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049) in view of Kaufmann (U.S. Patent No. 5,483,539).

With respect to claim 10, the Taborek, Sr. et al. reference teaches a serial to parallel converter for converting the serialized framed data to a parallel framed data (column 3, lines 17-25); and a guesser for guessing a position of a frame boundary in the output data word selected by the selector (column 5, line 61 – column 6, line 6). The Taborek, Sr. et al. reference does not teach a first register for receiving the parallel framed data from the serial to parallel converter and outputting a first output data word of the parallel framed data at a current cycle clock; a second register for receiving the first output data word, and outputting a second output data word corresponding to a previous first output data word from the first register of a previous cycle clock; a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output data word; a rotator for rotating the selected data word in accordance with the position guessed by the guesser; a third register for storing a previous version of the rotated data word; a select logic unit for combining a portion of the data word held in the rotator and a portion of data word held in the third register to

form a data output block comprising two or more synchronization patterns; a fourth register for storing the data output block; a tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns in the data output block; a counting mechanism coupled to the tester and being configured to count the number of valid and invalid synchronization patterns; and a state machine determining if the device is in a state of synchronization based on the counting mechanism, wherein said state machine is coupled to the third port of the selector and selectively provides the second output data word or the shifted data word to the guesser and the rotator. The Grivna reference teaches a first register for receiving the parallel framed data from the serial to parallel converter and outputting a first output data word of the parallel framed data at a current cycle clock (column 8, lines 49-57); a second register for receiving the first output data word, and outputting a second output data word corresponding to a previous first output data word from the first register of a previous cycle clock (column 8, lines 49-57); a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output data word (column 10, lines 44-56); a third register for storing a previous version of the rotated data word (see fig. 5, 596); a select logic unit for combining a portion of the data word held in the rotator and a portion of data word held in the third register to form a data output block comprising two or more synchronization patterns (see fig.5 and (column 10, line 44-column 11, line 12); fourth register for storing the data output block (see fig. 5,

580); a tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns in the data output block (column 10, lines 35-43) and (see fig. 5, 550 and 580) and a state machine determining if the device is in a state of synchronization based on the counting mechanism, wherein said state machine is coupled to the third port of the selector and selectively provides the second output data word or the shifted data word to the guesser and the rotator (column 11, line 26 – column 12, line 10). The Wright et al. reference teaches a rotator for rotating the selected data word in accordance with the position guessed by the guesser 9column 5, lines 42-53), (column 2, line 57 – column 3, line 10) and (column 3, lines 42-52). The Kaufman reference teaches a counting mechanism coupled to the tester and being configured to count the number of valid and invalid synchronization patterns (see fig. 5), (column 6, line 48 - column 7, line 4), (column 11, line 49 - column 12, line 2) and (column 12, lines 12-34). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al. and Grivna to incorporate a first register for receiving the parallel framed data from the serial to parallel converter and outputting a first output data word of the parallel framed data at a current cycle clock; a second register for receiving the first output data word, and outputting a second output data word corresponding to a previous first output data word from the first register of a previous cycle clock; a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output

data word; a third register for storing a previous version of the rotated data word; a select logic unit for combining a portion of the data word held in the rotator and a portion of data word held in the third register to form a data output block comprising two or more synchronization patterns; fourth register for storing the data output block and a state machine determining if the device is in a state of synchronization based on the counting mechanism, wherein said state machine is coupled to the third port of the selector and selectively provides the second output data word or the shifted data word to the guesser and the rotator into the claimed invention. The motivation for a first register for receiving the parallel framed data from the serial to parallel converter and outputting a first output data word of the parallel framed data at a current cycle clock; a second register for receiving the first output data word, and outputting a second output data word corresponding to a previous first output data word from the first register of a previous cycle clock; a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output data word; a third register for storing a previous version of the rotated data word; a select logic unit for combining a portion of the data word held in the rotator and a portion of data word held in the third register to form a data output block comprising two or more synchronization patterns; fourth register for storing the data output block and a state machine determining if the device is in a state of synchronization based on the counting mechanism, wherein said state machine is coupled to the third port of the selector and

selectively provides the second output data word or the shifted data word to the guesser and the rotator is for improved error recovery. Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al. and Grivna with Wright et al. to incorporate a rotator for rotating the selected data word in accordance with the position guessed by the guesser into the claimed invention. The motivation for a rotator for rotating the selected data word in accordance with the position guessed by the guesser is for improved system performance. Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al., Grivna and Wright et al. with Kaufman to incorporate a counting mechanism coupled to the tester and being configured to count the number of valid and invalid synchronization patterns into the claimed invention. The motivation for a counting mechanism coupled to the tester and being configured to count the number of valid and invalid synchronization patterns is for improved system performance.

With respect to claim 13, all of the limitations of claim 10 have been addressed above. The Taborek, Sr. et al. reference does not teach wherein the portion of the first output data word comprises first arriving serial bits of the parallel framed data at the current cycle clock and the portion of the second output data word comprises bits of the previous first output data word from the first register at the previous cycle clock starting at an offset of an odd number of bits from the first arriving bits. The Grivna reference teaches wherein the portion of the first output data word comprises first arriving serial

bits of the parallel framed data at the current cycle clock and the portion of the second output data word comprises bits of the previous first output data word from the first register at the previous cycle clock starting at an offset of an odd number of bits from the first arriving bits (column 10, lines 44-56). Thus, it would have been obvious to have combine the references Taborek, Sr. et al. and Grivna to incorporate wherein the portion of the first output data word comprises first arriving serial bits of the parallel framed data at the current cycle clock and the portion of the second output data word comprises bits of the previous first output data word from the first register at the previous cycle clock starting at an offset of an odd number of bits from the first arriving bits into the claimed invention. The motivation for wherein the portion of the first output data word comprises first arriving serial bits of the parallel framed data at the current cycle clock and the portion of the second output data word comprises bits of the previous first output data word from the first register at the previous cycle clock starting at an offset of an odd number of bits from the first arriving bits is for improved system performance.

With respect to claim 14, all of the limitations of claim 13 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the odd number of bits is one. The Wright et al. reference teaches wherein the odd number of bits is one (column 2, lines 46-56). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. reference and Wright et al. to incorporate wherein the odd number of bits is one into the

claimed invention. The motivation for wherein the odd number of bits is one is so cell delineation can be achieved. (Column 3, lines 50-51 – Wright et al. reference).

With respect to claim 15, the Taborek, Sr. et al. reference teaches wherein the serialized framed data comprises a plurality of frames, each frame comprising a data field and a synchronization pattern (column 8, lines 46-55).

With respect to claim 16, the Taborek, Sr. et al. reference teaches wherein the data field comprises 64b/66b (column 9, lines 10-27). The Taborek, Sr. et al. and Wright et al. references also addresses various aspects of ethernet technology that address field, synchronization, transmission and other aspects that make data field segmentation obvious to one skilled in the art.

With respect to claim 17, the Taborek, Sr. et al. reference teaches wherein the serialized data is a 10 Gb Ethernet data (column 2, line 55 – column 3, line 16).

With respect to claim 23, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the state of synchronization is obtained when the state machine detects a predetermined number of consecutive valid synchronization patterns in the serialized framed data. The Grivna reference teaches wherein the state of synchronization is obtained when the state machine detects a predetermined number of consecutive valid synchronization patterns in the serialized

framed data (column 11, line 49 – column 12, line 2). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Grivna to incorporate wherein the state of synchronization is obtained when the state machine detects a predetermined number of consecutive valid synchronization patterns in the serialized framed data into the claimed invention. The motivation for wherein the state of synchronization is obtained when the state machine detects a predetermined number of consecutive valid synchronization patterns in the serialized framed data is for improved system performance.

With respect to claim 25, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the width (or length) of the fourth register is greater than the width (or length) of the first, second, or third register. The Grivna reference teaches wherein the width (or length) of the fourth register is greater than the width (or length) of the first, second, or third register (see fig. 5). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Grivna to incorporate wherein the width (or length) of the fourth register is greater than the width (or length) of the first, second, or third register into the claimed invention. The motivation for wherein the width (or length) of the fourth register is greater than the width (or length) of the first, second, or third register is for improved system performance.

Claims 11-12 are rejected under Taborek, Sr. et al. (U.S. 7,0202,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049), Kaufmann (U.S. Patent No. 5,483,539) in view of Swoboda et al. (U.S. Patent No. 6,085,336).

With respect to claim 11, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser. The Swoboda et al. reference teaches an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser (column 38, lines 32-41). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser into the claimed invention. The motivation for an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

With respect to claim 12, all of the limitations of claim 11 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the guesser excludes the one or

more positions stored in the exhaust register as possible positions of the frame boundary. The Swoboda et al. reference teaches wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary (column 38, lines 58-65). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary into the claimed invention. The motivation for wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049), Kaufmann (U.S. Patent No. 5,483,539) in view of Fairchild et al. (U.S. Patent No. 5,508,955).

With respect to claim 21, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach a first counter for counting the number of valid synchronization patterns in the data output block and a second counter for counting the number of invalid synchronization patterns in the data output block. The Kaufmann reference teaches a first counter for counting the number of valid synchronization patterns in the data output block (column 6, line 48 - column 7, line 4), (column 11, line

49 - column 12, line 2) and (column 12, lines 12-34). The Fairchild et al. reference teaches and a second counter for counting the number of invalid synchronization patterns in the data output block (column 5, lines 37-56). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Kaufmann to incorporate a first counter for counting the number of valid synchronization patterns in the data output block into the claimed invention. The motivation for a first counter for counting the number of valid synchronization patterns in the data output block is for improved system performance. Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Fairchild et al. to incorporate and a second counter for counting the number of invalid synchronization patterns in the data output block into the claimed invention. The motivation for and a second counter for counting the number of invalid synchronization patterns in the data output block is for improved system performance.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049), Kaufmann (U.S. Patent No. 5,483,539) in view of Washington et al. (U.S. Patent No. 5,920,572).

With respect to claim 22, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the state machine resets the first and second counters when the state machine determines a change in the state of

synchronization. The Washington et al. reference teaches wherein the state machine resets the first and second counters when the state machine determines a change in the state of synchronization (column 11, lines 30-48). Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Washington et al. to incorporate wherein the state machine resets the first and second counters when the state machine determines a change in the state of synchronization into the claimed invention. The motivation for wherein the state machine resets the first and second counters when the state machine determines a change in the state of synchronization is for improved system performance.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049), Kaufmann (U.S. Patent No. 5,483,539) in view of Stephenson, Jr. et al. (U.S. Patent No. 5,081,654).

With respect to claim 24, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the first and second output data words are an integer multiple of eight (8) bits. The Stephenson, Jr. et al. reference teaches wherein the first and second output data words are an integer multiple of eight (8) bits (column 6, lines 9-23). Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. and Stephenson, Jr. et al. to incorporate wherein the first and second output data words are an integer multiple of eight (8) bits into the claimed invention. The motivation

for wherein the first and second output data words are an integer multiple of eight (8) bits is for improved system performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

12/8/09

/MUJTABA K CHAUDRY/

Primary Examiner, Art Unit 2112